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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,103	CHEN ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 15-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Reopening of Prosecution After Appeal Brief or Reply Brief

In view of the Appeal Brief filed on 8/31/06, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below.

JACK KEITH
SUPERVISORY PATENT EXAMINER

In response to Appellants' Appeal Brief filed 7/10/06 and again 8/31/06 prosecution is herewith re-opened in order to reduce possible issues for Appeal. Given the Amendment filed with said Appeal Brief said Amendment filed 7/10/06 is herewith entered (as confirmed in Advisory Action) and forms the basis for the following office action, in which apart from the withdrawal of the rejection under 35 USC 112, second paragraph, of claims 4, 18 and 22 (see section 2 thereof in the final office action under 35 USC 112, second paragraph), correction is made:

(a) in the Heading of the rejections under 35 USC 103(a) to include claim 24: claims 24 actually was rejected (see pages 16-17) in the previous final office action mailed 1/10/06;

(b) in that an objection to the Specification is included, because the Abstract apparently is incomplete as it ends with "and" and has no period at the end.

(c) despite the heading "Related Art" in the description of Figure 1 in the Specification, said Figure 1 is indicated as "Prior Art" and hence requires a Prior Art label.

(d) furthermore, an additional alternative rejection is provided with Prior Art as Admitted by Applicant as alternative to Sakui et al; and

(e) while applicant's arguments in traverse of the rejections under 35 USC 112, first paragraph, are in part persuasive in that "spaced alternately" when interpreted as "spaced one alongside the other" is in line with Merriam-Webster, and is disclosed (Figure 4), although this interpretation does not imply a patentable distinction over the prior art, as witnessed by a comparison between Figures 1A-1B in Hsu et al and Figure 4 of the Specification, and as explained formally in the rejections under 35 USC 103(a) of claims 19-22 now included.

For the above reasons the rejection is made non-final.

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to

avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

1. The abstract of the disclosure is objected to because the abstract ends with the word "and" and fails to have a period at the end. Correction is required. See MPEP § 608.01(b).

The following is a quotation from the relevant sections of the Patent Rules under 37 C.F.R. 1.75 that form the basis of the objection made in this office action.

(d)

(1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (see § 1.58(a)).

2. The Specification is objected to because the subject matter recited in original claims 3, 17 and 21 is not disclosed in the remainder of the Specification. This objection is provided subject to the noted indefiniteness under 35 USC 112, second paragraph and is based on an absence of any disclosure in the remainder of the specification on the thickness of the dielectric layers that separate the floating gates and select gates, and the dielectric layers that

separate the floating gates and the control gates, whether in absolute magnitudes or in relation to any other thickness.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. ***Claims 4, 18 and 22*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, claimed inter-gate capacitance "large enough for voltage coupling between the gates during program and erase operations" introduces an indefinite threshold beyond which the claimed inter-gate capacitance is "large enough" because the programs and erase operations are undefined in their characteristic magnitudes of voltages and time scales, i.e., the claimed program and erase operations have not been defined in quantitative electromagnetic terms and hence the conditions under which said voltage coupling exists is indefinite.
2. The term "relatively" in ***claim 3*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term

"relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

3. The term "relatively low" in ***claim 9*** is a relative term, which renders the claim indefinite. The term "relatively low voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
4. The term "relatively high" in ***claim 9*** is a relative term, which renders the claim indefinite. The term "relatively high positive voltage" (lines 2-3, 4, 5, 6-7 and 8) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
5. The term "relatively high" in ***claim 10*** is a relative term, which renders the claim indefinite. The term "relatively high negative voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
6. The term "relatively low" in ***claim 10*** is a relative term, which renders the claim indefinite. The term "relatively low negative voltage" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite

degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

7. The term "relatively high" in ***claim 11*** is a relative term, which renders the claim indefinite. The term "relatively high negative voltage" (line 2) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
8. The term "relatively low" in ***claim 11*** is a relative term, which renders the claim indefinite. The term "relatively low negative voltage" (lines 2-3) is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
9. The term "relatively" in ***claim 17*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.
10. The term "relatively" in ***claim 21*** as employed in three different places, namely: in "relatively thin" (line 1), in "first relatively thick" (line 2) and in "second relatively thick" (lines 3-4) is a relative term which renders the claim indefinite. The term "relatively" is not defined by the claim, the specification does not provide a

standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1-13 and 15-22*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (6,911,690 B2) (as previously made of record by examiner, see PTO-892) in view of either Prior Art as Admitted by Applicant and Chapman et al (6,118,161), and, - in an alternative rejection, over Sakui et al (6,411,548 B1) and Chapman et al (6,118,161).

Hsu et al teach a NAND flash memory cell array (Figures 1A, 1B, title, abstract and column 4, line 55 – column 6, line 24), comprising:

a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source region 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source region, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source region (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) positioned above a floating

gate 118 (column 5, line 36). Furthermore, a bitline diffusion, i.e., diffusion region for a bitline, inherently is contacted with a bitline, "bitline diffusion" being a diffusion region for contacting the bitline, thus requiring a bitline contact: both bitline and bitline contact must therefore exist; that the limitation "a bitline above the row, and a bit line contact interconnecting the bit line and the bit line diffusion" is inherent is also witnessed by Matas et al ("Memory 1997", by Integrated Circuit Engineering Corp., ISBN: 1-877750-59-X), Section 10, "Flash Memory Technology", pages 10-1 through 10-16, see especially page 10-5 on the NAND cell in Flash Memory chips, this review of the various memory devices including NAND flash memory chips showing a bitline bending down into a bitline contact contacting a bitline diffusion to the left of the leftmost select gate (Fig. 10-8) (N.B.: Matas et al is cited here for establishment of fact, not for teaching).

Hsu et al do not necessarily teach the last select gate in the row at least partially overlaps said source region. *However, it would have been obvious to include said limitation in view of either Prior Art as Admitted by Applicant (Figure 1 in the specification, see "Background of the Invention") or Sakui et al (Figure 47, and col. 27, lines 43-49),* who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region overlap (Figure 1 and legend (page 4) and pages 1-3 of the specification by applicants, and in the alternative: Figure 49 and column 27, lines 43-49 in Sakui et al) (with regard to Sakui et al: otherwise no overlap capacitance could exist). *Motivation* to include said teaching of overlap, between any select gate and source region derives from the well-known circumstance that for low resistance and good performance the gate should slightly

overlap with the source, as witnessed by Chapman et al (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any other MOS transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 2: clearly stacked gates and select gates are aligned to each other. The term "self-aligned" refers to the process of self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 3: This rejection is based on the assumption that the indefinite language of this claim may be interpreted to mean that the tunnel oxide is thinner than both the dielectric between the floating gate and the select gate and the dielectric between the floating gate and the control gate. The memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates and control gates. Hsu et al do not necessarily teach said first and second dielectric to be thick in comparison with said (necessarily thin) tunnel oxide. However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling, i.e., the explicit teaching of "tunnel oxide" means that the oxide layer is so thin that quantum-mechanically the layer can be crossed or penetrated although the charge carrier's energy is lower than the barrier

energy (see, e.g., Bohm, "Quantum Theory", 1951, ISBN: 0-486-65969-0; pages 238-240, cited for establishment of fact, not for teaching). Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 4: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates, in particular inter-gate capacitances between select gates and floating gates and between control gates and floating gates (see Figure 1B, showing said select and floating gates to be only a short distance apart, while having independent voltages, and showing said control gate and floating gates to be only a short distance apart, and having independent voltages. .

On claim 5: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted without giving weight to the limitation "high". Inherently, erase paths based on Fowler-Nordheim tunneling as exploited by Hsu et al extend from the floating gates, through the tunnel oxide to the channel regions by virtue of the very

existence of a current path for electrons between floating gate to the channel regions through Fowler-Nordheim tunneling (col. 8, l. 61-67), and voltage is coupled to the floating gates both from the control gates and from the select gates (keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin).

On claim 6: Program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates (because regions are conductive through the action of said gates, thereby allowing programming paths to exist); and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region (col. 3, l. 50-56): keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin. It is noted that the newly added limitations "below the floating gates" and "in the substrate" are met in any channel with lateral floating gates: the channel is located in the uppermost portion of the substrate abutting the interface between substrate and gate insulating layer. Therefore, said newly added limitations do nothing to further limit the cell array.

On claim 7: Program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates (because channel regions are highly conductive through the action of the gates and hence substantially conductive, thereby allowing programming paths to exist), while the remainder of the limitation defined by claim 7 constitutes functional language: In reference to the claim language

referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 8: The select gates in unselected cells *can be* biased at a relatively high voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source diffusion. Whether or not they are has no patentable weight: In reference to the claim language referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 9: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low positive voltage" and "relative high positive voltage" are terms merely indicating that the former voltage is lower than the latter voltage. The bit line for a row containing a selected cell to be programmed *can be*

held at 0 volts because said bit line is conductive; a relatively low positive voltage *can be* applied to a cell select gate for the selected cell as the select gates are independent; a relatively high positive voltage *can be* applied to the source diffusion at the second end of the row in which the selected cell is located because any source region is inherently conductive; a relatively high positive voltage *can be* applied to the control gate in the selected cell; a relatively high positive voltage *can be* applied to the select gates for unselected cells, and a relatively high positive voltage *can be* applied to the control gates in the unselected cells. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 10: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low negative voltage" and "relative high negative voltage" are terms merely indicating that the former voltage is lower in magnitude than the latter voltage. An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusions, the source diffusion and the P-well at 0 volts. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of

functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 11: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted assuming that "relatively low negative voltage" and "relative high negative voltage" are terms merely indicating that the former voltage is lower in magnitude than the latter voltage. An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the active area at a positive voltage and the bit line and source diffusions floating. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 12: A read path *can be* formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells (cell selection being possible in the structure defined by Figures 3 and 4a,b), with the common source at 0 volts, the bit line diffusion at 1-3 volts, and the control gate at relatively high positive

voltage, and the control gate of the selected cell *can be* biased at 0-1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state: application of a voltage on the control gate does improve the conductivity of the channel while for any non-vanishing conductivity in the channel and any non-zero voltage on the bitline diffusion relative to the source region a positive amount of current is known to flow between bitline and source: inherently so, because electrons in the channel respond to the positive gate voltage by forming a thin layer of enhanced conductivity along the connection between source and drain (bitline diffusion), i.e., a conduction channel under the floating gate. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 13: As discussed under claim 11, an erase path *can be* formed by biasing of control gates and select gates; since this biasing can be done for each individual member in the cell array an erase path can erase the whole cell array simultaneously; and since cells can be selected individually a program path which is single cell selectable *can be* created through appropriate biasing. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional

language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 15: Hsu et al teach a NAND flash memory cell array (Figures 1A, 1B, title, abstract and column 4, line 55 – column 6, line 24), comprising:

a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source diffusion 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source diffusion (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) positioned above a floating gate 118 (column 5, line 36). Furthermore, a bitline diffusion, i.e., diffusion region for a bitline, inherently is contacted with a bitline: both bitline and bitline contact, if only in the form of a contact interface, must therefore exist; that the limitation "a bitline above the row, and a bit line contact interconnecting the bit line and the bit line diffusion" is inherent is also witnessed by Matas et al ("Memory 1997", by Integrated Circuit Engineering Corp., ISBN: 1-877750-59-X), Section 10, "Flash Memory Technology", pages 10-1 through 10-16, see especially page 10-5 on the NAND cell in Flash Memory chips, this review of the various memory devices including NAND flash

memory chips showing a bitline bending down into a bitline contact contacting a bitline diffusion to the left of the leftmost select gate (Fig. 10-8).

Hsu et al do not necessarily teach the last select gate in the row being directly above said source region. *However, it would have been obvious to include said limitation in view of Sakui et al,* who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region showing said select gate directly above said source diffusion (i.e., a vertical line may be drawn intersecting both source diffusion and select gate (Figure 49; see also column 27, lines 43-49) (otherwise no overlap capacitance could exist). *Motivation* to include said teaching derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by Chapman et al (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 16: clearly stacked gates 118/122 and select gates 106 are aligned to each other (see Figures 1A and 1B). The term "self-aligned" refers to the process of "self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 17: the memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates

and control gates. Hsu et al do not necessarily teach said first and second dielectric to be thick in comparison with said (necessarily thin) tunnel oxide. However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling. Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 18: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates; , in particular inter-gate capacitances between select gates and floating gates and between control gates and floating gates (see Figure 1B, showing said select and floating gates to be only a short distance apart, while having independent voltages, and showing said control gate and floating gates to be only a short distance apart, and having independent voltages.

On claim 19: Hsu et al teach a NAND flash memory cell array, comprising: a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), bit line

diffusions 124 (col. 5, l. 63) and source diffusions 126 (col. 5, l. 65) spaced alternately ("alternately" here interpreted as "arranged one alongside the other") in the active area with no other diffusions between them, a plurality of stacked gates 118/120 (col. 5, l. 3-5) and select gates 106 (col. 5, l. 27) arranged alternately ("alternately" here interpreted as "arranged one alongside the other") in rows between the bitline diffusions and the source diffusions (Figure 1A), with each of the stacked gates having a control gate 120 (col. 5, l. 27) positioned above a floating gate 118 (col. 5, l. 36). Furthermore, any bit line diffusion is inherently in contact with a bit contact and bit line contacts interconnecting the bit lines and bit line diffusions (diffusion being a region in the substrate wherein impurities have been diffused to establish a region of elevated electrical conductivity so as to serve as electrical contact to the bit line), as seen, for instance from the description and definition of the prior art through Figure 1 in the Specification (see pages 1-3 and Figure 1 in the Specification); that the limitation "a bitline above the row, and a bit line contact interconnecting the bit line and the bit line diffusion" is inherent is also witnessed by Matas et al ("Memory 1997", by Integrated Circuit Engineering Corp., ISBN: 1-877750-59-X), Section 10, "Flash Memory Technology", pages 10-1 through 10-16, see especially page 10-5 on the NAND cell in Flash Memory chips, this review of the various memory devices including NAND flash memory chips showing a bitline bending down into a bitline contact contacting a bitline diffusion to the left of the leftmost select gate (Fig. 10-8).

Hsu et al do not necessarily teach "the last select gates in each of the rows at least partially overlapping the source diffusions between the rows".

However, it would have been obvious to include said limitation in view of either Prior Art as Admitted by Applicant (Figure 1 in the specification, see "Background of the Invention") or Sakui et al (Figure 47, and col. 27, lines 43-49), who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region overlap (Figure 1 and legend (page 4) and pages 1-3 of the specification by applicants, and in the alternative: Figure 49 and column 27, lines 43-49 in Sakui et al) (with regard to Sakui et al: otherwise no overlap capacitance could exist). *Motivation* to include said teaching of overlap, between any select gate and source region derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by the teaching of *Chapman et al* (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 20: clearly stacked gates and select gates are aligned to each other. The term "self-aligned" refers to the process of self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 21: the memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates

and control gates. Hsu et al do not necessarily teach said first and second dielectric to be thick in comparison with said (necessarily thin) tunnel oxide. However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling. (see, e.g., Bohm, "Quantum Theory", 1951, ISBN: 0-486-65969-0; pages 238-240, cited for establishment of fact, not for teaching). Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 22: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates, in particular inter-gate capacitances between select gates and floating gates and between control gates and floating gates (see Figure 1B, showing said select and floating gates to be only a short distance apart, while having independent voltages, and showing said control gate and floating gates to be only a short distance apart, and having independent voltages.

On claim 24: *Hsu et al teach*:

a NAND flash memory cell array, comprising: a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source diffusion 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source diffusion (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) and a floating gate 118 (column 5, line 36) with aligned sides adjacent to the select gates (Figure 1B), erase paths between the floating gates and channel regions in the active area beneath the stacked gates (col. 8, lines 61-67).

The limitation "self-aligned" rather than merely "aligned" only further introduces a limitation on the method of making said memory cell array and fails to further limit the invention claimed here as a final structure only. The distinction between "aligned" and "self-aligned" thus constitutes a product-by-process limitation and is non-limiting. A product by process limitation is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Furthermore, voltage coupling from the control gates to the floating gates inherently exists because the control gates control by definition the voltage of the floating gates so as to control the number of charge carriers in said floating gates while voltage coupling between select gates and floating gates inherently exists because the select gates determine whether or not a channel exists along which charge carriers can approach said floating gates.

Response to Arguments

(1) Applicant's argument in traverse of rejection under 35 USC 112, second paragraph, of claims 19-22, is persuasive in that "alternately" in one meaning, albeit not in the usual meaning of alternately in the art, found in the dictionary does appear to be disclosed by applicant, namely "arranged one alongside the other". Therefore, the rejection under 112, 1st paragraph, of claims 19-22 has been withdrawn.

(2) Although the intergate capacitances are now defined, what is "large enough to couple voltages between floating gates and select gates and between floating gates and control gates" depends on the magnitude and time scales of the voltages which have not been defined. Accordingly, claims 4, 18 and 22 are still rejected under 35 USC 112, second paragraph, in amended form.

Applicant is furthermore reminded that the magnitude of voltages and their time scales depend on intended use. In reference to the claim language cited above, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of

performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). Accordingly, claims 4, 18 and 22 are still rejected under 35 USC 112m second paragraph, even in amended form.

(3) With regard to the traverse of the rejection under 35 USC 103(a) of claims 1-13, 15-18, and 24 applicant underrates what is inherent in a NAND Flash Memory cell array, as witnessed for instance by Matas et al in their introduction to NAND Flash Memory Technology, showing bitline diffusion (horizontal overhead portion of component marked "Bitline", and bitline contact (vertically inclined portion of said component) contacting bitline diffusion in the substrate (Figure 10-8 and discussion thereof). Applicant's traverse of the use of Chapman is not persuasive because the NAND flash memory cell array transistors are MOSFET transistors (see 10-1 in Matas et al reciting gate oxide), thus specifically teaching MOS (metal-oxide-semiconductor (silicon) field effect transistors). What would have been obvious for the individual MOSFET. Therefore, said traverse does not persuade. Moreover, with the interpretation of "alternate" as defined overleaf, claims 19-22 are rejected over the same references (see rejections under 35 USC 103(a) above).

(a) On further comments of traverse with regard to claim 1 specifically (page 7): Counter to applicant's allegation the prior art as cited shows (Hsu et al) a bit line diffusion and source region in the active area of the substrate with no other diffusions in the active area between bit line diffusion and source region (see Hsu et al, Figure 1B). a plurality of stacked gates (select and control gates being stacked, the latter on the former) and arranged "one alongside the other" (which is the only possible meaning of

"alternately" as disclosed in the specification; compare in this regard Figure 4 of the specification with Figure 1A in Hsu et al and noting that 126 is laterally abutting the last stacked gate 118/120 in the row). Furthermore, please note the teaching by Mata et al in this regard on what is a defining description of NAND Flash Memory technology (see above under Claim Rejections under 35 USC 103(a)).

(b) On further comments in traverse specifically for claim 3, applicant does not explain why there is no basis for the cost incentive as cited. However, if the peculiar difficulties and consequent costs of reliably establishing a tunnel oxide are not clear from knowledge in the art, reference is made to Duffy et al to establish the recognition of said difficulties and associated cost (see especially the first paragraph of the Introduction section) (Duffy et al, "Advanced Process Development using Numerical Simulation", in "Advanced MOS and Bi-Polar Devices", IEE Colloquium, London 2/14//1995, pages 14/1 – 14/6).

(c) On further comments in traverse of the rejection of claim 9, applicant in his argument does not address the stated reason for not attaching patentable weight to the limitations as cited, which were provided with the rejection, i.e., the functional language only limits intended use.

(d) On comments in traverse of the rejection of claim 12, the claim language does not specify any quantitative characteristic of the erase and program operation that limits either the conductivity of the channel or the current through said channel, and hence the capability as cited in the rejection is correct.

(e) On comments in traverse of the rejection of claim 15, these comments refer to those ("noted above") made on claim 1, which fail to persuade for the same reasons as noted above in this action (see comments on claim 1 ad a).

For the above reasons the art rejections are maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
November 13, 2006

~~Supervisory~~ Primary Patent Examiner: